

AMENDMENTS TO THE CLAIMS

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1. (Presently Amended) A memory integrated circuit comprising:
one or more data input/output terminals;
an input buffer ~~register~~; and
a state decoder for receiving a chip select signal targeted for the memory integrated circuit; and
a bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer ~~register~~,
wherein the switch is an integral part of the memory integrated circuit, and wherein the ~~memory integrated circuit input buffer~~ input buffer is selectively decoupled from the terminals from the bus in response to a change in state in the chip select signal, and wherein the switch is operated so as to control the parasitic capacitance of the terminals.
 2. (Presently Amended) A memory integrated circuit comprising:
a contact which connects to a data bus; and
a switch, wherein an input portion of said switch is connected to said contact,
wherein the switch is operated so as to control the parasitic capacitance of the terminals.
 3. (Presently Amended) The integrated circuit of Claim 2 wherein an output portion of said switch is connected to one or more buffers ~~buffer registers~~.
 4. (Presently Amended) A memory integrated circuit comprising:
one or more data input/output terminals;
an input buffer ~~register~~; and
a bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer wherein the switch is operated so as to control the parasitic capacitance of the input/output terminals ~~register~~; and
one or more control terminals for receiving memory access control signals, and
wherein ~~said~~ a logic circuit is coupled to at least one of said one or more control terminals.
 5. (Original) The memory integrated circuit of Claim 4, wherein said bus switch further comprises a control portion coupled to a logic circuit on said memory integrated circuit,

where in said logic circuit is configured to selectively open said bus switch during at least a portion of a memory access cycle.

6. (Original) The memory integrated circuit of Claim 4, wherein said memory integrated circuit further comprises one or more control terminals for receiving memory access control signals, and wherein said logic circuit is coupled to at least one of said one or more control terminals.

7. (Presently Amended) A memory integrated circuit comprising:
one or more data input/output terminals;
an input buffer ~~register~~; and
a bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer ~~register~~,
wherein the switch is an integral part of the memory integrated circuit, wherein the switch is operated so as to control the parasitic capacitance of the input/output terminals; and
one or more control terminals for receiving memory access control signals, and
wherein a ~~said~~ logic circuit is coupled to at least one of said one or more control terminals.

8. (Presently Amended) A memory integrated circuit comprising:
one or more data input/output terminals;
an input buffer ~~register~~;
a state decoder for receiving a ~~chip~~ chip select signal targeted for the memory circuit;
a bus switch having an input portion connected to said one or more data input/output terminals, and an output portion connected to said input buffer ~~register~~,
wherein the input buffer ~~memory integrated circuit~~ is selectively decoupled from the bus in response to a change in state in the chip select signal, wherein the switch is operated so as to control the parasitic capacitance of the input/output terminals; and
one or more control terminals for receiving memory access control signals, and
wherein a ~~said~~ logic circuit is coupled to at least one of said one or more control terminals.

9. (Presently Amended) A method of transferring data, the method comprising:
disabling a transfer gate when no memory access are occurring ~~occurring~~;

enabling a transfer gate ~~gate~~ when memory accesses are ~~occurring~~ occurring,
wherein the transfer gate is operated so as to control the parasitic capacitance of a bus;

wherein enabling and disabling occur in a memory integrated circuit.

10. (Presently Amended) The method of Claim 9, wherein the memory integrated circuit additionally comprises a contact which connects to a data bus and a switch, wherein an input portion of said switch is connected to the contact, wherein an output portion of said switch is connected to one or more buffer buffers ~~registers~~, the method further comprising, transferring data to and from the buffers subsequent to enabling the transfer gate.

11. (Presently Amended) A system for transferring data, the system comprising:

means for disabling a transfer gate when no memory access are occurring ~~occurring~~;

means for enabling a transfer gate when memory accesses are occurring ~~occurring~~,
wherein the switch is operated so as to control the parasitic capacitance of a bus; and

wherein the means for enabling and the means for disabling reside within a memory integrated circuit.

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